WHAT IS CLAIMED IS:

1. A self-directing bus amplifier circuit comprising:

a. an input biased at a given voltage level;

b. a tri-state amplifier having a first input terminal coupled to said biased input and having an output coupled to an output bus;

c. a field effect transistor having a gate terminal coupled to said biased input, a source terminal coupled to ground potential, and a drain terminal coupled to an inhibiting input of said amplifier; and

d. said drain terminal of said field effect transistor coupled to a source of voltage for bias thereof, such that when a signal is present on said input said field effect transistor turns OFF, which enables said tri-state amplifier so that said signal is passed through to said output bus.

2. The circuit as in Claim 1 wherein said field effect transistor is an N channel device.

3. The circuit as in Claim 1 wherein said tri-state amplifier is an OP AMP having an inhibiting input thereof.

4. The circuit as in Claim 1 wherein said input is biased at a given level by means of a resistor coupled between said input and source voltage.

5. The circuit as in Claim 1 wherein said drain terminal of said field effect transistor is biased at a given level by means of a resistor coupled between said drain terminal and source voltage.

6. The circuit as in Claim 1 wherein a resistor is coupled between the output of said tri-state amplifier and said output bus for controlling the output impedance of said self-directing amplifier.

7. The circuit as in Claim 1 wherein a gain network is coupled between a second input terminal of said tri-state amplifier and the output thereof.

8. A self-directing bus amplifier circuit comprising:

a. an input biased at a given voltage level;

b. a tri-state amplifier having a first input terminal coupled to said biased input and having an output coupled to an output bus;

c. a field effect transistor having a gate terminal coupled to said biased input, a source terminal coupled to ground potential, and a drain terminal coupled to an inhibiting input of said amplifier; and

d. said drain terminal of said field effect transistor coupled to a source of voltage for bias thereof, such that when a signal is present on said input said field effect transistor turns OFF, which enables said tri-state amplifier so that said signal is passed through to said output bus;

e. wherein said input is biased at a given level by means of a resistor coupled between said input and source voltage.

9. The circuit as in Claim 8 wherein said field effect transistor is an N channel device.

10. The circuit as in Claim 8 wherein said tri-state amplifier is an OP AMP having an inhibiting input thereof.

11. The circuit as in Claim 8 wherein said drain terminal of said field effect transistor is biased at a given level by means of a resistor coupled between said drain terminal and source voltage.

12. The circuit as in Claim 8 wherein a resistor is coupled between the output of said tri-state amplifier and said output bus for controlling the output impedance of said self-directing amplifier.

13. The circuit as in Claim 8 wherein a gain network is coupled between a second input terminal of said tri-state amplifier and the output thereof.

14. A self-directing bus amplifier circuit comprising:

a. an input biased at a given voltage level;

b. a tri-state amplifier having a first input terminal coupled to said biased input and having an output coupled to an output bus;

c. a field effect transistor having a gate terminal coupled to said biased input, a source terminal coupled to ground potential, and a drain terminal coupled to an inhibiting input of said amplifier; and

d. said drain terminal of said field effect transistor coupled to a source of voltage for bias thereof, such that when a signal is present on said input said field effect transistor turns OFF, which enables

said tri-state amplifier so that said signal is passed through to said output bus;

e. wherein said input is biased at a given level by means of a resistor coupled between said input and source voltage; and

f. wherein said drain terminal of said field effect transistor is biased at a given level by means of a resistor coupled between said drain terminal and source voltage.

15. The circuit as in Claim 14 wherein said field effect transistor is an N channel device.

16. The circuit as in Claim 14 wherein said tri-state amplifier is an OP AMP having an inhibiting input thereof.

17. The circuit as in Claim 14 wherein a resistor is coupled between the output of said tri-state amplifier and said output bus for controlling the output impedance of said self-directing amplifier.

18. The circuit as in Claim 14 wherein a gain network is coupled between a second input terminal of said tri-state amplifier and the output thereof.

19. In a video matrix routing switcher, a method for isolating a source of video signals on an input bus from an output bus, said method comprising:

a. providing an input biased at a given voltage level;

b. coupling a tri-state amplifier having a first input terminal between said biased input and an output bus;

c. coupling a gate terminal of a field effect transistor to said biased input, coupling a source terminal thereof to ground potential, and coupling a drain terminal to an inhibiting input of said amplifier;

d. coupling said drain terminal of said field effect transistor to a source of voltage for bias thereof;

e. providing a signal on said input, which turns off said field effect transistor thereby enabling said tri-state amplifier so that said signal is passed through to said output bus.

20. The circuit method as in Claim 19 wherein said input is biased at a given level by means of coupling a resistor between said input and source voltage.

21. The circuit method as in Claim 19 wherein said drain terminal of said field effect transistor is biased at a given level by means of coupling a resistor between said drain terminal and source voltage.

22. The circuit method as in Claim 19 further comprising the step of coupling a resistor between the output of said tri-state amplifier and said output bus for controlling the output impedance of said self-directing amplifier.

23. The circuit method as in Claim 19 further comprising the step of coupling a gain network between a second input terminal of said tri-state amplifier and the output thereof.